

EPROM/ROM-Based 8-Bit Microcontroller Series

Devices Included in this Data Sheet:

 FM8PS54E/S56E : EPROM devices FM8PS54/S56: Mask ROM devices

FEATURES

- · Only 42 single word instructions
- · All instructions are single cycle except for program branches which are two-cycle
- · 13-bit wide instructions
- · All ROM/EPROM area GOTO instruction
- All ROM/EPROM area subroutine CALL instruction
- · 8-bit wide data path
- 5-level deep hardware stack
- · Operating speed: DC-20 MHz clock input

DC-100 ns instruction cycle

Device	Pins #	I/O #	EPROM/ROM (Byte)	RAM (Byte)								
FM8PS54/S54E	18	16	512	49								
FM8PS56/S56E	18	16	1K	49								

- · Direct, indirect addressing modes for data accessing
- · 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler
- Internal Power-on Reset (POR)
- Built-in Low Voltage Detector (LVD) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer(OST)
- · On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- Two I/O ports IOA and IOB with independent direction control (maximum 16 I/O pins)
- Soft-ware I/O pull-high/pull-down or open-drain control
- · One internal interrupt source: Timer0 overflow; Two external interrupt source: INT pin, Port B input change
- · Wake-up from SLEEP by INT pin or Port B input change
- Power saving SLEEP mode
- · Built-in 8MHz, 4MHz, 1MHz, and 455KHz internal RC oscillator
- · Programmable Code Protection
- · Selectable oscillator options:
 - ERC: External Resistor/Capacitor Oscillator
 - HF: High Frequency Crystal/Resonator Oscillator
 - XT: Crystal/Resonator Oscillator
 - LF: Low Frequency Crystal Oscillator
 - IRC: Internal Resistor/Capacitor Oscillator
 - ERIC: External Resistor/Internal Capacitor Oscillator
- · Wide-operating voltage range:
 - EPROM: 2.3V to 5.5V - ROM: 2.3V to 5.5V

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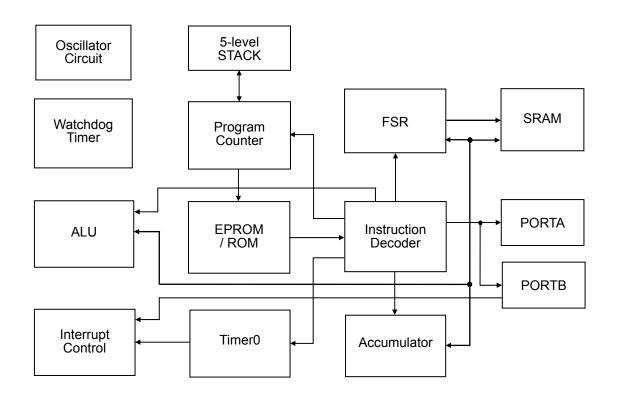
GENERAL DESCRIPTION

The FM8PS54/S56 series is a family of low-cost, high speed, high noise immunity, EPROM/ROM-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 42 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.

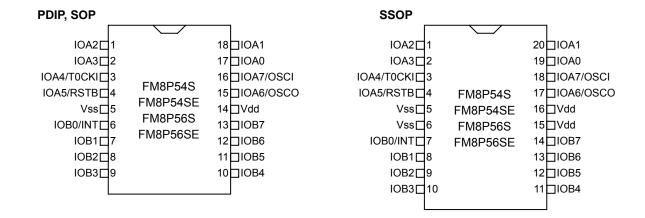
The FM8PS54/S56 series consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Oscillator Start-up Timer(OST), Watchdog Timer, EPROM/ROM, SRAM, tri-state I/O port, I/O pull-high/open-drain/pull-down control, Power saving SLEEP mode, real time programmable clock/counter, Interrupt, Wake-up from SLEEP mode, and Code Protection for EPROM products. There are three oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. The FM8PS54/S54E address 512×13 of program memory, and the FM8PS56/S56E address 1K×13 of program memory.

The FM8PS54/S56 can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTIONS

Name	I/O	Description
IOA0 ~ IOA7	I/O	IOA0 ~ IOA7 as bi-direction I/O port, and IOA5 is an input only pin.
IOB0/INT	I/O	Bi-direction I/O pin with system wake-up function / External interrupt input
IOB1 ~ IOB7	I/O	Bi-direction I/O port with system wake-up function
T0CKI		Clock input to Timer0. Must be tied to Vss or Vdd, if not in use, to reduce current
TUCKI	1	consumption
RSTB	1	System clear (RESET) input. This pin is an active low RESET to the device.
OSCI		X'tal type: Oscillator crystal input
0301	1	RC type: Clock input of RC oscillator
osco	0	X'tal type: Oscillator crystal output.
0300	0	RC mode: Outputs with the instruction cycle rate
Vdd	-	Positive supply
Vss	1	Ground

Legend: I=input, O=output, I/O=input/output

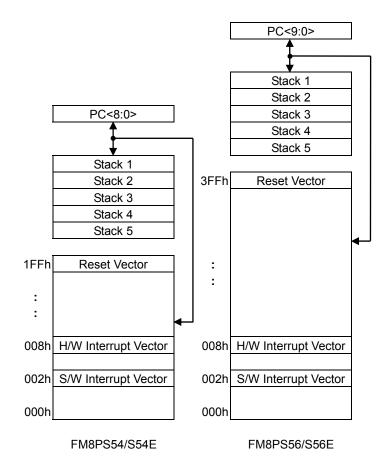
1.0 MEMORY ORGANIZATION

FM8PS54/S56 memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8PS54/S54E have a 9-bit Program Counter (PC) capable of addressing a 512×13 program memory space. The FM8PS56/S56E have a 10-bit Program Counter capable of addressing a 1K×13 program memory space. The RESET vector for the FM8PS54/S54E is at 1FFh. The RESET vector for the FM8PS56/S56E is at 3FFh. The H/W interrupt vector is at 008h. And the S/W interrupt vector is at 002h. FM8PS54/S56 supports all ROM/EPROM area CALL/GOTO instructions without page.

FIGURE 1.1: Program Memory Map and STACK



1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.

The General Purpose Registers are accessed either directly or indirectly through the FSR register.

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.

TABLE 1.1: Registers File Map for FM8P54/56 Series

<u></u>	ABLE 1.1. Registers i lie map for i mor 54,00 denes									
Address	Description									
00h	INDF									
01h	TMR0									
02h	PCL									
03h	STATUS									
04h	FSR									
05h	PORTA									
06h	PORTB									
07h	General Purpose Register									
08h	PCON									
09h	WUCON									
0Ah	PCHBUF									
0Bh	PDCON									
0Ch	ODCON									
0Dh	PHCON									
0Eh	INTEN									
0Fh	INTFLAG									
10h ~ 3Fh	General Purpose Registers									

N/A OPTION

05h	IOSTA
06h	IOSTB

TABLE 1.2: The Registers Controlled by OPTION or IOST Instructions

	ALL THE REGISTER CONTROLLER BY CT HERE OF THE HIGH GOLDING												
Address	Name	В7	В6	B5	B4	В3	B2	B1	В0				
N/A (w)	OPTION	-	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0				
05h (w)	IOSTA		Port A I/O Control Register										
06h (w)	IOSTB			Po	rt B I/O Co	ntrol Regis	ter						

TABLE 1.3: Operational Registers Map

	operational i										
Address	Name	B7	В6	B5	B4	В3	B2	B1	В0		
00h (r/w)	INDF	Us	Uses contents of FSR to address data memory (not a physical register)								
01h (r/w)	TMR0		8-bit real-time clock/counter								
02h (r/w)	PCL		Low order 8 bits of PC								
03h (r/w)	STATUS	GP2	GP1	GP0	TO	PD	Z	DC	С		
04h (r/w)	FSR	*	* * Indirect data memory address pointer								
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0		
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0		
07h (r/w)	SRAM	General Purpose Register									
08h (r/w)	PCON	WDTE	EIS	LVDTE	ROC	-	-	-	-		
09h (r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0		
0Ah (r/w)	PCHBUF (2)	-	-	ı	-	-		2 MSBs B	uffer of PC		
0Bh (r/w)	PDCON	/PDB3	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0		
0Ch (r/w)	ODCON	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0		
0Dh (r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4	/PHB3	/PHB2	/PHB1	/PHB0		
0Eh (r/w)	INTEN	GIE	-	-	-	-	INTIE	PBIE	TOIE		
0Fh (r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF		

Legend: - = unimplemented, read as '0', * = unimplemented, read as '1'

Note 1: There is only 1 bit in FM8PS54/S54E. And there are 2 bits in FM8PS56/S56E.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

Address	Name	В7	B6	B5	B4	В3	B2	B1	В0		
00h (r/w)	INDF	Use	Uses contents of FSR to address data memory (not a physical register)								

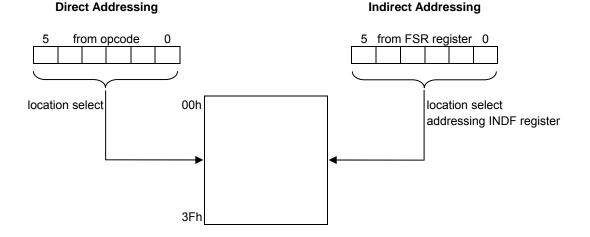
The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

The bits 5-0 of FSR register are used to select up to 64 registers (address: 00h ~ 3Fh).

EXAMPLE 2.1: INDIRECT ADDRESSING

- · Register file 38 contains the value 10h
- Register file 39 contains the value 0Ah
- · Load the value 38 into the FSR Register
- · A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (@FSR=39h)
- · A read of the INDR register now will return the value of 0Ah.

FIGURE 2.1: Direct/Indirect Addressing



2.1.2 TMR0 (Time Clock/Counter register)

Address	Name	B7	В6	B5	B4	В3	B2	B1	В0
01h (r/w)	TMR0			8-b	it real-time	clock/cour	nter		

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the instruction cycle clock or by an external clock source (T0CKI pin) defined by T0CS bit (OPTION<5>). If T0CKI pin is selected, the Timer0 is increased by T0CKI signal rising/falling edge (selected by T0SE bit (OPTION<4>)).

The prescaler is assigned to Timer0 by clearing the PSA bit (OPTION<3>). In this case, the prescaler will be cleared when TMR0 register is written with a value.

2.1.3 PCL (Low Bytes of Program Counter) & Stack

Address	Name	B7	B6	B5	B4	В3	B2	B1	B0
02h (r/w)	PCL				Low order 8	B bits of PC	;		

FM8PS54/S56 devices have a 9-bit (for FM8PS54/S54E) or 10-bit (for FM8PS56/S56E) wide Program Counter (PC) and five-level deep 9-bit (or 10-bit) hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<9:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCHBUF register. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC. For a GOTO instruction, the PC<9:0> is provided by the GOTO instruction word. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.

For a CALL instruction, the PC<9:0> is provided by the CALL instruction word. The next PC will be loaded (PUSHed) onto the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated. For a RETIA, RETFIE, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.

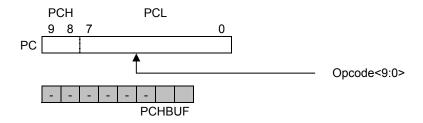
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result. However, the PC<9:8> will come from the PCHBUF<1:0> bits (PCHBUF \rightarrow PCH).

PCHBUF register is never updated with the contents of PCH.

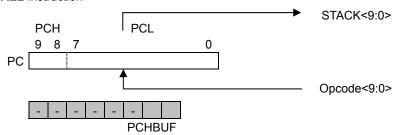


FIGURE 2.2: Loading of PC in Different Situations

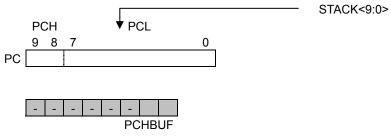
Situation 1: GOTO Instruction



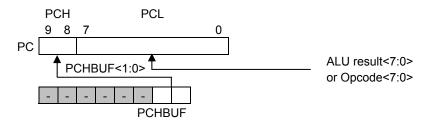
Situation 2: CALL Instruction



Situation 3: RETIA, RETFIE, or RETURN Instruction



Situation 4: Instruction with PCL as destination



Note: 1. Bits PC<9> and PCHBUF<1> are unimplemented for FM8PS54/S54E.

2. PCHBUF is used only for instruction with PCL as destination for FM8PS54/S54E/56/S56E.

2.1.4 STATUS (Status Register)

P	Address	Name	B7	В6	B5	B4	В3	B2	B1	В0
0)3h (r/w)	STATUS	GP2	GP1	GP0	TO	PD	Z	DC	С

This register contains the arithmetic status of the ALU, the RESET status.

If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the <u>write</u> to <u>these</u> three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C: Carry/borrow bit.

ADDAR, ADDIA

- = 1, a carry occurred.
- = 0, a carry did not occur.

SUBAR, SUBIA

- = 1, a borrow did not occur.
- = 0, a borrow occurred.

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC: Half carry/half borrow bit.

ADDAR, ADDIA

- = 1, a carry from the 4th low order bit of the result occurred.
- = 0, a carry from the 4th low order bit of the result did not occur.

SUBAR, SUBIA

- = 1, a borrow from the 4th low order bit of the result did not occur.
- = 0, a borrow from the 4th low order bit of the result occurred.

Z: Zero bit.

- = 1, the result of a logic operation is zero.
- = 0, the result of a logic operation is not zero.

PD: Power down flag bit.

- = 1, after power-up or by the CLRWDT instruction.
- = 0, by the SLEEP instruction.

TO: Time overflow flag bit.

- = 1, after power-up or by the CLRWDT or SLEEP instruction.
- = 0, a watch-dog time overflow occurred.

GP2:GP0: General purpose read/write bits.

2.1.5 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	В3	B2	B1	B0
04h (r/w)	FSR	*	*		Indirect	data memo	ory address	pointer	

Bit5:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

Bit7:Bit6: Not used. Read as "1"s.

2.1.6 PORTA & PORTB (Port Data Registers)

Address	Name	В7	В6	B5	B4	В3	B2	B1	В0
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Reading the port (PORTA, PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch.

PORTA and PORTB are 8-bit port data Registers.

2.1.7 PCON (Power Control Register)

Address	Name	В7	В6	B5	B4	В3	B2	B1	В0
08h (r/w)	PCON	WDTE	EIS	LVDTE	ROC	-	-	-	-

Bit3:Bit0: Not used. Read as "0"s.

ROC: R-option function of IOA0 and IOA1 pins enable bit.

- = 0, Disable the R-option function.
- = 1, Enable the R-option function. In this case, if a 430KΩ external resister is connected/disconnected to Vss, the status of IOA0 (IOA1) is read as "0"/"1".

LVDTE: LVDT (low voltage detector) enable bit.

- = 0, Disable LVDT.
- = 1, Enable LVDT.

EIS: Define the function of IOB0/INT pin.

- = 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
- = 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to "1". The path of Port B input change of IOB0 pin is masked by hardware, the status of INT pin can also be read by way of reading PORTB.

WDTE: WDT (watch-dog timer) enable bit.

- = 0, Disable WDT.
- = 1, Enable WDT.

2.1.8 WUCON (Port B Input Change Interrupt/Wake-up Control Register)

Add	ress	Name	В7	В6	B5	B4	В3	B2	B1	В0
09h	(r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

WUB0: = 0, Disable the input change interrupt/wake-up function of IOB0 pin.

= 1, Enable the input change interrupt/wake-up function of IOB0 pin.

WUB1: = 0, Disable the input change interrupt/wake-up function of IOB1 pin.

= 1, Enable the input change interrupt/wake-up function of IOB1 pin.

WUB2: = 0, Disable the input change interrupt/wake-up function of IOB2 pin.

= 1, Enable the input change interrupt/wake-up function of IOB2 pin.

WUB3: = 0, Disable the input change interrupt/wake-up function of IOB3 pin.

= 1, Enable the input change interrupt/wake-up function of IOB3 pin.

WUB4: = 0, Disable the input change interrupt/wake-up function of IOB4 pin.



= 1, Enable the input change interrupt/wake-up function of IOB4 pin.

WUB5: = 0, Disable the input change interrupt/wake-up function of IOB5 pin.

= 1, Enable the input change interrupt/wake-up function of IOB5 pin.

WUB6: = 0, Disable the input change interrupt/wake-up function of IOB6 pin.

= 1, Enable the input change interrupt/wake-up function of IOB6 pin.

WUB7: = 0, Disable Enable the input change interrupt/wake-up function of IOB7 pin.

= 1, Enable the input change interrupt/wake-up function of IOB7 pin.

2.1.9 PCHBUF (High Byte Buffer of Program Counter)

ĺ	Address	Name	B7	В6	B5	B4	В3	B2	B1	В0
I	0Ah (r/w)	PCHBUF	-	-	-	-	-		2 MSBs B	uffer of PC

There is only 1 bit in FM8PS54/S54E/55/55E. And there are 2 bits in FM8PS56/S56E. See 2.1.3 for detail description.

2.1.10 PDCON (Pull-down Control Register)

Address	Name	B7	B6	B5	B4	В3	B2	B1	В0
0Bh (r/w)	PDCON	/PDB3	/PDB2	/PDB1	/PDB0	/PDA3	/PDA2	/PDA1	/PDA0

/PDA0 : = 0, Enable the internal pull-down of IOA0 pin.

= 1, Disable the internal pull-down of IOA0 pin.

/PDA1: = 0, Enable the internal pull-down of IOA1 pin.

= 1, Disable the internal pull-down of IOA1 pin.

/PDA2: = 0, Enable the internal pull-down of IOA2 pin.

= 1, Disable the internal pull-down of IOA2 pin.

/PDA3: = 0, Enable the internal pull-down of IOA3 pin.

= 1, Disable the internal pull-down of IOA3 pin.

/PDB0: = 0, Enable the internal pull-down of IOB0 pin.

= 1, Disable the internal pull-down of IOB0 pin.

/PDB1: = 0, Enable the internal pull-down of IOB1 pin.

= 1, Disable the internal pull-down of IOB1 pin.

/PDB2 : = 0, Enable the internal pull-down of IOB2 pin.

= 1, Disable the internal pull-down of IOB2 pin.

/PDB3 : = 0, Enable the internal pull-down of IOB3 pin.

= 1, Disable the internal pull-down of IOB3 pin.



2.1.11 ODCON (Open-drain Control Register)

Address	Name	B7	В6	B5	B4	В3	B2	B1	В0
0Ch (r/w)	ODCON	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0

ODB0: = 0, Disable the internal open-drain of IOB0 pin.

= 1, Enable the internal open-drain of IOB0 pin.

ODB1: = 0, Disable the internal open-drain of IOB1 pin.

= 1, Enable the internal open-drain of IOB1 pin.

ODB2: = 0, Disable the internal open-drain of IOB2 pin.

= 1, Enable the internal open-drain of IOB2 pin.

ODB3: = 0, Disable the internal open-drain of IOB3 pin.

= 1, Enable the internal open-drain of IOB3 pin.

ODB4: = 0, Disable the internal open-drain of IOB4 pin.

= 1, Enable the internal open-drain of IOB4 pin.

ODB5: = 0, Disable the internal open-drain of IOB5 pin.

= 1, Enable the internal open-drain of IOB5 pin.

ODB6: = 0, Disable the internal open-drain of IOB6 pin.

= 1, Enable the internal open-drain of IOB6 pin.

ODB7: = 0, Disable the internal open-drain of IOB7 pin.

= 1, Enable the internal open-drain of IOB7 pin.

2.1.12 PHCON (Pull-high Control Register)

Address	Name	B7	B6	B5	B4	В3	B2	B1	В0
0Dh (r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4	/PHB3	/PHB2	/PHB1	/PHB0

/PHB0 : = 0, Enable the internal pull-high of IOB0 pin.

= 1, Disable the internal pull-high of IOB0 pin.

/PHB1: = 0, Enable the internal pull-high of IOB1 pin.

= 1, Disable the internal pull-high of IOB1 pin.

/PHB2: = 0, Enable the internal pull-high of IOB2 pin.

= 1, Disable the internal pull-high of IOB2 pin.

/PHB3 : = 0, Enable the internal pull-high of IOB3 pin.

= 1, Disable the internal pull-high of IOB3 pin.

/PHB4 : = 0, Enable the internal pull-high of IOB4 pin.

= 1, Disable the internal pull-high of IOB4 pin.

/PHB5 : = 0, Enable the internal pull-high of IOB5 pin.

= 1, Disable the internal pull-high of IOB5 pin.

/PHB6: = 0, Enable the internal pull-high of IOB6 pin.

= 1, Disable the internal pull-high of IOB6 pin.



/PHB7: = 0, Enable the internal pull-high of IOB7 pin.

= 1, Disable the internal pull-high of IOB7 pin.

2.1.13 INTEN (Interrupt Mask Register)

Address	Name	В7	В6	B5	B4	В3	B2	B1	В0
0Eh (r/w)	INTEN	GIE	-	-	-	-	INTIE	PBIE	T0IE

T0IE: Timer0 overflow interrupt enable bit.

- = 0, Disable the Timer0 overflow interrupt.
- = 1, Enable the Timer0 overflow interrupt.

PBIE: Port B input change interrupt enable bit.

- = 0, Disable the Port B input change interrupt.
- = 1, Enable the Port B input change interrupt .

INTIE: External INT pin interrupt enable bit.

- = 0, Disable the External INT pin interrupt.
- = 1, Enable the External INT pin interrupt.

Bit6:BIT3: Not used. Read as "0"s.

GIE: Global interrupt enable bit.

- = 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction.
- = 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (008h).

Note: When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

2.1.14 INTFLAG (Interrupt Status Register)

Address	Name	B7	В6	B5	B4	В3	B2	B1	В0
0Fh (r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

T0IF: Timer0 overflow interrupt flag. Set when Timer0 overflows, reset by software.

PBIF: Port B input change interrupt flag. Set when Port B input changes, reset by software.

INTIF: External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (OPTION<6>)) edge on INT pin, reset by software.

Bit7:BIT3: Not used. Read as "0"s.

2.1.15 ACC (Accumulator)

Address	Name	В7	В6	B5	B4	В3	B2	B1	В0
N/A (r/w)	ACC				Accum	nulator			

Accumulator is an internal data transfer, or instruction operand holding. It can not be addressed.

2.1.16 OPTION Register

ı	Address	Name	В7	В6	B5	B4	В3	B2	B1	В0
	N/A (w)	OPTION	-	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Accessed by OPTION instruction.

By executing the OPTION instruction, the contents of the ACC Register will be transferred to the OPTION Register. The OPTION Register is a 7-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler, Timer0, and the external INT interrupt.

The OPTION Register are "write-only" and are set all "1"s except INTEDG bit.

PS2:PS0: Prescaler rate select bits.

PS2:PS0	Timer0 Rate	WDT Rate
0 0 0	1:2	1:1
0 0 1	1:4	1:2
0 1 0	1:8	1:4
0 1 1	1:16	1:8
1 0 0	1:32	1:16
1 0 1	1:64	1:32
1 1 0	1:128	1:64
1 1 1	1:256	1:128

PSA: Prescaler assign bit.

= 1, WDT (watch-dog timer).

= 0, TMR0 (Timer0).

T0SE: TMR0 source edge select bit.

= 1, Falling edge on T0CKI pin.

= 0, Rising edge on T0CKI pin.

T0CS: TMR0 clock source select bit.

= 1, External T0CKI pin.

= 0, internal instruction clock cycle.

INTEDG: Interrupt edge select bit.

= 1, interrupt on rising edge of INT pin.

= 0, interrupt on falling edge of INT pin.

Bit7: Not used.

2.1.17 IOSTA, & IOSTB (Port I/O Control Registers)

Add	lress	Name	В7	В6	B5	B4	В3	B2	B1	В0
N/A	(w)	IOSTA		Port A I/O Control Register						
N/A	۱ (w)	IOSTB		Port B I/O Control Register						

Accessed by IOST instruction.

The Port I/O Control Registers are loaded with the contents of the ACC Register by executing the IOST R (05h~06h) instruction. A '1' from a IOST Register bit puts the corresponding output driver in hi-impedance state (input mode). A '0' enables the output buffer and puts the contents of the output data latch on the selected pins (output mode). The IOST Registers are "write-only" and are set (output drivers disabled) upon RESET.

2.2 I/O Ports

Port A and port B are bi-directional tri-state I/O ports. Port A and Port B are 8-pin I/O ports. Port C is a general purpose register. Please note that IOA5 is an input only pin.

All I/O pins (IOA<7:0> and IOB<7:0>) have data direction control registers (IOSTA, IOSTB) which can configure these pins as output or input.

IOB<7:0> have its corresponding pull-high control bits (PHCON register) to enable the weak internal pull-high. The weak pull-high is automatically turned off when the pin is configured as an output pin.

IOA<3:0> and IOB<3:0> have its corresponding pull-down control bits (PDCON register) to enable the weak internal pull-down. The weak pull-down is automatically turned off when the pin is configured as an output pin.

IOB<7:0> have its corresponding open-drain control bits (ODCON register) to enable the open-drain output when these pins are configured to be an output pin.

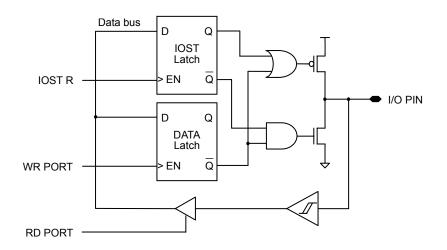
IOA0 and IOA1 are the R-option pins enabled by setting the ROC bit (PCON<4>). When the R-option function is used, it is recommended that IOA0 and IOA1 are used as output pins, and read the status of IOA0 and IOA1 before these pins are configured to be an output pin.

IOB<7:0> also provides the input change interrupt/wake-up function. Each pin has its corresponding input change interrupt/wake-up enable bits (WUCON) to select the input change interrupt/wake-up source.

The IOB0 is also an external interrupt input signal by setting the EIS bit (PCON<6>). In this case, IOB0 input change interrupt/wake-up function will be disabled by hardware even if it is enabled by software.

FIGURE 2.3: Block Diagram of I/O PINs

IOA7, IOA6, IOA4 ~ IOA0:



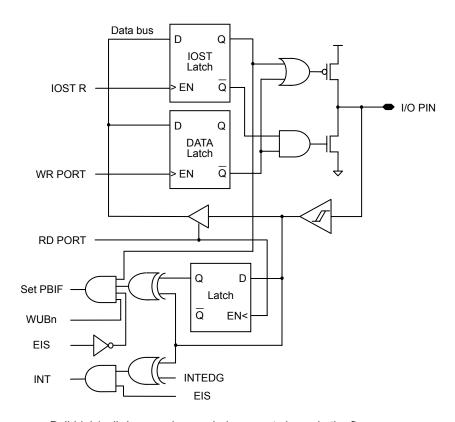
Pull-down is not shown in the figure

IOA5:



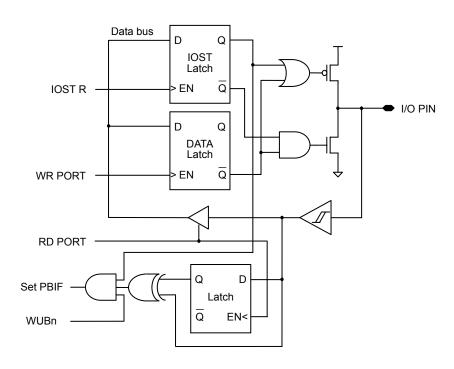


IOB0/INT:



Pull-high/pull-down and open-drain are not shown in the figure

IOB7 ~ IOB1 :



Pull-high/pull-down and open-drain are not shown in the figure



2.3 Timer0/WDT & Prescler

2.3.1 Timer0

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the internal clock or by an external clock source (T0CKI pin).

2.3.1.1 Using Timer0 with an Internal Clock: Timer mode

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the timer0 register (TMR0) will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles.

2.3.1.2 Using Timer0 with an External Clock: Counter mode

Counter mode is selected by setting the T0CS bit (OPTON<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).

The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least $2 \, T_{OSC}$ and low for at least $2 \, T_{OSC}$.

When a prescaler is used, the external clock input is divided by the asynchronous prescaler. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc divided by the prescaler value.

2.3.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the TO bit (STATUS<4>) will be cleared.

The WDT can be disabled by clearing the control bit WDTE (PCON<7>) to "0".

The WDT has a nominal time-out period of 18 ms (without prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the OPTION register. Thus, the longest time-out period is approxmately 2.3 seconds.

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device reset.

The SLEEP instruction resets the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

2.3.3 Prescaler

An 8-bit counter (down counter) is available as a prescaler for the Timer0, or as a postscaler for the Watchdog Timer (WDT). Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 means that there is no prescaler for the WDT, and vice-versa.

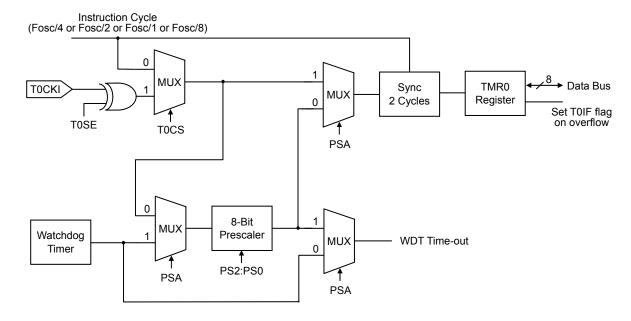
The PSA bit (OPTION<3>) determines prescaler assignment. The PS<2:0> bits (OPTION<2:0>) determine prescaler ratio.

When the prescaler is assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler. When it is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '1's.

To avoid an unintended device reset, CLRWDT or CLRR TMR0 instructions must be executed when changing the prescaler assignment from Timer0 to the WDT, and vice-versa.



FIGURE 2.4: Block Diagram of The Timer0/WDT Prescaler



2.4 Interrupts

The FM8PS54/S56 series has up to three sources of interrupt:

- 1. External interrupt INT pin.
- 2. TMR0 overflow interrupt.
- Port B input change interrupt (pins IOB7:IOB0).

INTFLAG is the interrupt flag register that recodes the interrupt requests in the relative flags.

A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.

When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 008h.

The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.

The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.

The flag bit (except PBIF bit) in INTFLAG register is set by interrupt event regardless of the status of its mask bit. Reading the INTFLAG register will be the logic AND of INTFLAG and INTEN.

When an interrupt is generated by the INT instruction, the next instruction will be fetched from address 002h.

2.4.1 External INT Interrupt

External interrupt on INT pin is rising or falling edge triggered selected by INTEDG (OPTION<6>).

When a valid edge appears on the INT pin the flag bit INTIF (INTFLAG<2>) is set. This interrupt can be disabled by clearing INTIE bit (INTEN<2>).

The INT pin interrupt can wake-up the system from SLEEP condition, if bit INTIE was set before going to SLEEP. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

2.4.2 Timer0 Interrupt

An overflow (FFh \rightarrow 00h) in the TMR0 register will set the flag bit T0IF (INTFLAG<0>). This interrupt can be disabled by clearing T0IE bit (INTEN<0>).



2.4.3 Port B Input Change Interrupt

An input change on IOB<7:0> set flag bit PBIF (INTFLAG<1>). This interrupt can be disabled by clearing PBIE bit (INTEN<1>).

Before the port B input change interrupt is enabled, reading PORTB (any instruction accessed to PORTB, including read/write instructions) is necessary. Any pin which corresponding WUBn bit (WUCON<7:0>) is cleared to "0" or configured as output or IOB0 pin configured as INT pin will be excluded from this function.

The port B input change interrupt also can wake-up the system from SLEEP condition, if bit PBIE was set before going to SLEEP. And GIE bit also decides whether or not the processor branches to the interrupt vector following wake-up. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

2.5 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

When SLEEP instruction is executed, the \overrightarrow{PD} bit (STATUS<3>) is cleared, the \overrightarrow{TO} bit is set, the watchdog timer will be cleared and keeps running, and the oscillator driver is turned off.

All I/O pins maintain the status they had before the SLEEP instruction was executed.

2.5.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:

- 1. RSTB reset.
- 2. WDT time-out reset (if enabled).
- 3. Interrupt from RB0/INT pin, or PORTB change interrupt.

External RSTB reset and WDT time-out reset will cause a device reset. The \overline{PD} and \overline{TO} bits can be used to determine the cause of device reset. The \overline{PD} bit is set on power-up and is cleared when SLEEP instruction is executed. The \overline{TO} bit is cleared if a WDT time-out occurred.

For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set. Wake-up is regardless of the GIE bit. If GIE bit is cleared, the device will continue execution at the instruction after the SLEEP instruction. If the GIE bit is set, the device will branch to the interrupt address (008h).

The system wake-up delay time is 18ms plus 128 oscillator cycle time.

2.6 Reset

FM8PS54/S56 devices may be RESET in one of the following ways:

- 1. Power-on Reset (POR)
- 2. Brown-out Reset (BOR)
- 3. RSTB Pin Reset
- 4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a "reset state" on Power-on Reset, RSTB or WDT Reset.

A Power-on RESET pulse is generated on-chip when Vdd rise is detected. To use this feature, the user merely ties the RSTB pin to Vdd.

On-chip Low Voltage Detector (LVD) places the device into reset when Vdd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation Vdd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.

A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.6.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 18ms delay after Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active. The PWDT delay will vary from device to device due to Vdd, temperature, and process variation.

2.6.2 Oscillator Start-up Timer(OST)

The OST timer provides a 128 oscillator cycle delay (from OSCI input) after the PWRT delay (18ms) is over. This delay ensures that the X'tal oscillator or resonator has started and stabilized. The device is kept in reset state as long as the OST is active.

This counter only starts incrementing after the amplitude of the OSCI signal reaches the oscillator input thresholds.

2.6.3 Reset Sequence

When Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset is detected, the reset sequence is as follows:

- 1. The reset latch is set and the PWRT & OST are cleared.
- 2. When the internal POR, BOR, RSTB Reset or WDT time-out Reset pulse is finished, then the PWRT begins counting.
- 3. After the PWRT time-out, the OST is activated.
- 4. And after the OST delay is over, the reset latch will be cleared and thus end the on-chip reset signal.

The totally system reset delay time is 18ms plus 128 oscillator cycle time.

FIGURE 2.5: Simplified Block Diagram of on-chip Reset Circuit

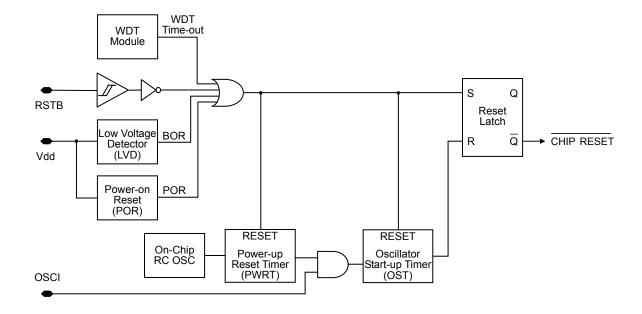


TABLE 2.1: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
OPTION	N/A	-011 1111	-011 1111
IOSTA	05h	1111 1111	1111 1111
IOSTB	06h	1111 1111	1111 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
FSR	04h	11xx xxxx	11uu uuuu
PORTA	05h	xxxx xxxx	uuuu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
General Purpose Register	07h	xxxx xxxx	uuuu uuuu
PCON	08h	1010	1010
WUCON	09h	0000 0000	0000 0000
PCHBUF	0Ah	54:0 56:00	54:0 56:00
PDCON	0Bh	1111 1111	1111 1111
ODCON	0Ch	0000 0000	0000 0000
PHCON	0Dh	1111 1111	1111 1111
INTEN	0Eh	0000	0000
INTFLAG	0Fh	000	000
General Purpose Registers	10 ~ 3Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented,

= refer to the following table for possible values.

TABLE 2.2: TO/PD Status after Reset

TO	PD	RESET was caused by
1	1	Power-on Reset
1	1	Brown-out reset
u	u	RSTB Reset during normal operation
1	0	RSTB Reset during SLEEP
0	1	WDT Reset during normal operation
0	0	WDT Reset during SLEEP

Legend: u = unchanged

TABLE 2.3: Events Affecting TO/PD Status Bits

Event	TO	PD
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged



2.7 Hexadecimal Convert to Decimal (HCD)

Decimal format is another number format for FM8PS54/S56. When the content of the data memory has been assigned as decimal format, it is necessary to convert the results to decimal format after the execution of ALU instructions. When the decimal converting operation is processing, all of the operand data (including the contents of the data memory (RAM), accumulator (ACC), immediate data, and look-up table) should be in the decimal format, or the results of conversion will be incorrect.

Instruction DAA can convert the ACC data from hexadecimal to decimal format after any addition operation and restored to ACC.

The conversion operation is illustrated in example 2.2.

EXAMPLE 2.2: DAA CONVERSION

MOVIA	90h	;Set immediate data = decimal format number "90" (ACC ← 90h)
MOVAR	30h	;Load immediate data "90" to data memory address 30H
MOVIA	10h	;Set immediate data = decimal format number "10" (ACC ← 10h)
ADDAR	30h, 0	;Contents of the data memory address 30H and ACC are binary-added
		;the result loads to the ACC (ACC \leftarrow A0h, C \leftarrow 0)
DAA		;Convert the content of ACC to decimal format, and restored to ACC
		;The result in the ACC is "00" and the carry bit C is "1". This represents the
		;decimal number "100"

Instruction DAS can convert the ACC data from hexadecimal to decimal format after any subtraction operation and restored to ACC.

The conversion operation is illustrated in example 2.3.

EXAMPLE 2.3: DAS CONVERSION

٠.	*** LL 2.5. L		21101011
	MOVIA	10h	;Set immediate data = decimal format number "10" (ACC ← 10h)
	MOVAR	30h	;Load immediate data "10" to data memory address 30H
	MOVIA	20h	;Set immediate data = decimal format number "20" (ACC ← 20h)
	SUBAR	30h, 0	;Contents of the data memory address 30H and ACC are binary-subtracted
			;the result loads to the ACC (ACC ← F0h, C ← 0)
	DAS		;Convert the content of ACC to decimal format, and restored to ACC
			;The result in the ACC is "90" and the carry bit C is "0". This represents the
			;decimal number " -10"

2.8 Oscillator Configurations

FM8PS54/S56 can be operated in six different oscillator modes. Users can program three configuration bits (Fosc<2:0>) to select the appropriate modes:

- ERC: External Resistor/Capacitor Oscillator
- · HF: High Frequency Crystal/Resonator Oscillator
- XT: Crystal/Resonator Oscillator
- · LF: Low Frequency Crystal Oscillator
- IRC: Internal Resistor/Capacitor Oscillator
- ERIC: External Resistor/Internal Capacitor Oscillator

In LF, XT, or HF modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, XT, or HF modes, the devices can have an external clock source drive the OSCI pin. The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the resistor (Rext) and capacitor (Cext), the operating temperature, and the process parameter.

The IRC/ERIC device option offers largest cost savings for timing insensitive applications. These devices offer 4 different internal RC oscillator frequency, 8MHz, 4MHz, 1MHz, and 455KHz, which is selected by two configuration bits (RCM<1:0>). Or user can change the oscillator frequency with external resistor. The ERIC oscillator frequency is a function of the resistor (Rext), the operating temperature, and the process parameter.

FIGURE 2.6: HF, XT, or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

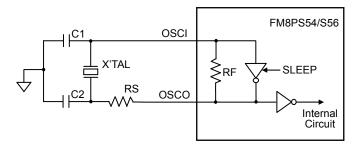


FIGURE 2.7: HF, XT, or LF Oscillator Modes (External Clock Input Operation)

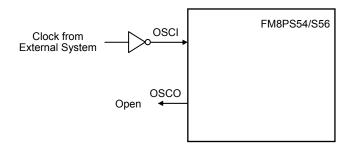




FIGURE 2.8: ERC Oscillator Mode

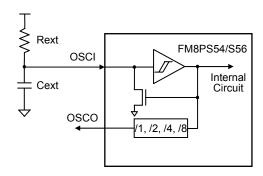


FIGURE 2.9: IRC Oscillator Mode (Internal R, Internal C Oscillator)

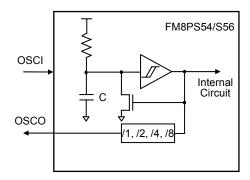
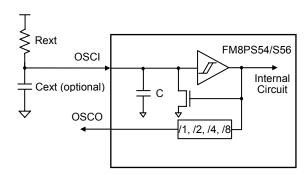


FIGURE 2.10: ERIC Oscillator Mode (External R, Internal C Oscillator)





2.9 Configurations Word

TABLE 2.4: Configurations Word 0

Name	Description
	Oscillator Selection Bits
	= 1, 1, 1 → ERC mode (external R & C) (default);
	IOA6/OSCO pin controlled by OSCOUT configuration bit
	= 1, 1, 0 → HF mode
F000	= 1, 0, 1 → XT mode
Fosc	= 1, 0, 0 → LF mode
	= 0, 1, 1 → IRC mode (internal R & C);
	IOA6/OSCO pin controlled by OSCOUT configuration bit
	= 0, 1, 0 → ERIC mode (external R & internal C);
	IOA6/OSCO pin controlled by OSCOUT configuration bit
	Watchdog Timer Enable Bit
WDTEN	= 1, WDT enabled (default)
	= 0, WDT disabled
	Code Protection Bit
PROTECT	= 1, EPROM code protection off (default)
	= 0, EPROM code protection on
	Low Voltage Detector Selection Bit
	= 1, 1 → disable (default)
LVDT	= 1, 0 → enable, LVDT voltage = 2.0V, controlled by SLEEP
	= 0, 1 → enable, LVDT voltage = 2.0V
	= 0, 0 → enable, LVDT voltage = 3.6V
	Instruction Period Selection Bits
OSCD	= 1, 1 → four oscillator periods (default)
ОООВ	= 1, 0 → two oscillator periods
	= 0, 0 → eight oscillator periods
	IRC/ERIC Mode Selection Bits
	= 1, 1 → 4MHz (default)
RCM	= 1, 0 → 8MHz
	= 0, 1 → 1MHz
	= 0, 0 → 455KHz
	IOA6/OSCO Pin Selection Bit for ERC/IRC/ERIC Mode
OSCOUT	= 1, OSCO pin is selected; Instruction clock will be output (default)
	= 0, IOA6 pin is selected
	IOA5/RSTB Pin Selection Bit
RSTBIN	= 1, IOA5 pin is selected (default)
	= 0, RSTB pin is selected

TABLE 2.5: Configurations Word 1

Name	Description			
CAL	Calibration Selection Bits for IRC Mode			
	Power Mode Selection Bit			
PMOD	= 1, Non-power saving (default)			
	= 0, Power saving			
	Read Port Control bit for Output Pins			
RDPORT	= 1, From registers (default)			
	= 0, From pins			
	Wake-up & Subsequest-Resets Timer for ERC/IRC/ERIC modes			
RCT	= 1, 140us (default)			
	= 0, 18ms			



3.0 INSTRUCTION SET

Mnemo Opera		Description	Operation	Cycles	Status Affected
BCR	R, bit	Clear bit in R	0 → R 	1	1
BSR	R, bit	Set bit in R	1 → R 	1	-
BTRSC	R, bit	Test bit in R, Skip if Clear	Skip if R = 0	1/2 (1)	-
BTRSS	R, bit	Test bit in R, Skip if Set	Skip if R = 1	1/2 (1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	TO, PD
OPTION		Load OPTION register	ACC → OPTION	1	-
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	\overline{TO}_{p}
INT		S/W interrupt	PC + 1 → Top of Stack, 002h → PC	2	-
DAA		Adjust ACC's data format from HEX to DEC after any addition operation	ACC(hex) → ACC(dec)	1	С
DAS		Adjust ACC's data format from HEX to DEC after any subtraction operation	ACC(hex) → ACC(dec)	1	-
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	00h → ACC	1	Z
IOST	R	Load IOST register	ACC → IOST register	1	-
CLRR	R	Clear R	00h → R	1	Z
MOVAR	R	Move ACC to R	ACC → R	1	-
MOVR	R, d	Move R	R → dest	1	Z
DECR	R, d	Decrement R	R - 1 → dest	1	Z
DECRSZ	R, d	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2 (1)	-
INCR	R, d	Increment R	R + 1 → dest	1	Z
INCRSZ	R, d	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2 (1)	-
ADDAR	R, d	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	R, d	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	R, d	Add ACC and R with Carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	R, d	Subtract ACC from R with Carry	R + ACC + C → dest	1	C, DC, Z
ANDAR	R, d	AND ACC with R	ACC and R → dest	1	Z
IORAR	R, d	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	R, d	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	R, d	Complement R	R → dest	1	Z
RLR	R, d	Rotate left f through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	С



RRR	R, d	Rotate right f through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	С
SWAPR	R, d	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	I	Move Immediate to ACC	I → ACC	1	-
ADDIA	I	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	I	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	I	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	I	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	I	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA	ı	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	ı	Call subroutine	PC + 1 → Top of Stack, I → PC<9:0>	2	-
GOTO	I	Unconditional branch	I → PC<9:0>	2	-

Note: 1. 2 cycles for skip, else 1 cycle

2. bit : Bit address within an 8-bit register R

R: Register address (00h to 3Fh)

I : Immediate data ACC : Accumulator d : Destination select;

=0 (store result in ACC)

=1 (store result in file register R)

dest : Destination PC : Program Counter

PCHBUF: High Byte Buffer of Program Counter

WDT: Watchdog Timer Counter GIE: Global interrupt enable bit

 $\overline{\frac{\text{TO}}{\text{PD}}}$: Time-out bit PD : Power-down bit

C: Carry bit

DC : Digital carry bit

Z : Zero bit



ADCAR Add ACC and R with Carry

Syntax: ADCAR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: $R + ACC + C \rightarrow dest$

Status Affected: C, DC, Z

Description: Add the contents of the ACC register and register 'R' with Carry. If 'd' is 0 the result is stored

in the ACC register. If 'd' is '1' the result is stored back in register 'R'.

Cycles: 1

ADDAR Add ACC and R

Syntax: ADDAR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: $ACC + R \rightarrow dest$

Status Affected: C, DC, Z

Description: Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC

register. If 'd' is '1' the result is stored back in register 'R'.

Cycles: 1

ADDIA Add ACC and Immediate

Syntax: ADDIA I
Operands: $0 \le I \le 255$ Operation: ACC + I \rightarrow ACC

Status Affected: C, DC, Z

Description: Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the

ACC register.

Cycles: 1

ANDAR AND ACC and R

Syntax: ANDAR R, d Operands: $0 \le R \le 63$

 $d\!\in\![0,\!1]$

Operation: ACC and $R \rightarrow dest$

Status Affected: Z

Description: The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in

the ACC register. If 'd' is '1' the result is stored back in register 'R'.

Cycles: 1

ANDIA AND Immediate with ACC

Syntax: ANDIA I Operands: $0 \le I \le 255$

Operation: ACC AND I → ACC

Status Affected: Z

Description: The contents of the ACC register are AND'ed with the 8-bit immediate 'l'. The result is placed

in the ACC register.



BCR Clear Bit in R

Syntax: BCF R, b Operands: $0 \le R \le 63$ $0 \le b \le 7$

0 → R

Status Affected: None

Description: Clear bit 'b' in register 'R'.

Cycles: 1

Operation:

BSR Set Bit in R

Syntax: BSR R, b Operands: $0 \le R \le 63$

 $0 \le b \le 7$ Operation: $1 \to R < b >$

Status Affected: None

Description: Set bit 'b' in register 'R'.

Cycles: 1

BTRSC Test Bit in R, Skip if Clear

Syntax: BTRSC R, b Operands: $0 \le R \le 63$

 $0 \le b \le 7$

Operation: Skip if R < b > = 0

Status Affected: None

Description: If bit 'b' in register 'R' is 0 then the next instruction is skipped.

If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded,

and a NOP is executed instead making this a 2-cycle instruction..

Cycles: 1(2)

BTRSS Test Bit in R, Skip if Set

Syntax: BTRSS R, b Operands: $0 \le R \le 63$ $0 \le b \le 7$ Operation: Skip if R
b> = 1

Status Affected: None

Description: If bit 'b' in register 'R' is '1' then the next instruction is skipped.

If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is

discarded and a NOP is executed instead, making this a 2-cycle instruction.

Cycles: 1(2)

CALL Subroutine Call

Syntax: CALL I Operands: $0 \le I \le 1023$

Operation: PC +1 \rightarrow Top of Stack;

I → PC<9:0>

PCHBUF<2> → PC<10>

Status Affected: None

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The 10-bit immediate

address is loaded into PC bits <9:0>. CALL is a two-cycle instruction.



CLRA Clear ACC

Syntax: CLRA Operands: None

Operation: $00h \rightarrow ACC$;

 $1 \rightarrow Z$

Status Affected: Z

Description: The ACC register is cleared. Zero bit (Z) is set.

Cycles: 1

CLRR Clear R

Syntax: CLRR R
Operands: $0 \le R \le 63$ Operation: $00h \rightarrow R$; $1 \rightarrow Z$

Status Affected: Z

Description: The contents of register 'R' are cleared and the Z bit is set.

Cycles: 1

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Operands: None

Operation: $00h \rightarrow WDT$;

00h → WDT prescaler (if assigned);

1 → TO; 1 → PD

Status Affected: TO PD

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is

assigned to the WDT and not Timer0. Status bits TO and PD are set.

Cycles: 1

COMR Complement R

Syntax: COMR R, d Operands: $0 \le R \le 63$ $d \in [0,1]$ Operation: $R \to dest$

Status Affected: Z

Description: The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC

register. If 'd' is 1 the result is stored back in register 'R'.

Cycles: 1

DAA Adjust ACC's data format from HEX to DEC

Syntax: DAA Operands: None

Operation: $ACC(hex) \rightarrow ACC(dec)$

Status Affected: C

Description: Convert the ACC data from hexadecimal to decimal format after any addition

operation and restored to ACC.



DAS Adjust ACC's data format from HEX to DEC

Syntax: DAS Operands: None

Operation: $ACC(hex) \rightarrow ACC(dec)$

Status Affected: None

Description: Convert the ACC data from hexadecimal to decimal format after any subtraction operation

and restored to ACC.

Cycles: 1

DECR Decrement R

Syntax: DECR R, d Operands: $0 \le R \le 63$ $d \in [0,1]$

Operation: $R - 1 \rightarrow dest$

Status Affected: Z

Description: Decrement register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is

stored back in register 'R'.

Cycles: 1

DECRSZ Decrement R, Skip if 0

Syntax: DECRSZ R, d Operands: $0 \le R \le 63$ $d \in [0,1]$

Operation: $R - 1 \rightarrow dest$; skip if result =0

Status Affected: None

Description: The contents of register 'R' are decremented. If 'd' is 0 the result is placed in the ACC

register. If 'd' is 1 the result is placed back in register 'R'.

If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is

executed instead making it a two-cycle instruction.

Cycles: 1(2)

GOTO Unconditional Branch

Syntax: GOTO I Operands: $0 \le I \le 1023$ Operation: $I \rightarrow PC < 9:0 >$

PCHBUF<2> → PC<10>

Status Affected: None

Description: GOTO is an unconditional branch. The 10-bit immediate value is loaded into PC bits <9:0>.

GOTO is a two-cycle instruction.

Cycles: 2

INCR Increment R

Syntax: INCR R, d

Operands: $0 \le R \le 63$ $d \in [0,1]$ Operation: $R + 1 \rightarrow dest$

Status Affected: Z

Description: The contents of register 'R' are incremented. If 'd' is 0 the result is placed in the ACC register.

If 'd' is 1 the result is placed back in register 'R'.



INCRSZ Increment R, Skip if 0

Syntax: INCRSZ R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: $R + 1 \rightarrow dest$, skip if result = 0

Status Affected: None

Description: The contents of register 'R' are incremented. If 'd' is 0 the result is placed in the ACC register.

If 'd' is the result is placed back in register 'R'.

If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is

executed instead making it a two-cycle instruction.

Cycles: 1(2)

INT S/W Interrupt

Syntax: INT Operands: None

Operation: $PC + 1 \rightarrow Top \text{ of Stack}$,

002h → PC

Status Affected: None

Description: Interrupt subroutine call. First, return address (PC+1) is pushed onto the stack. The address

002h is loaded into PC bits <9:0>.

Cycles: 2

IORAR OR ACC with R

Syntax: IORAR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: ACC or R → dest

Status Affected: Z

Description: Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC

register. If 'd' is 1 the result is placed back in register 'R'.

Cycles: 1

IORIA OR Immediate with ACC

Syntax: IORIA I
Operands: $0 \le I \le 255$ Operation: ACC or I \rightarrow ACC

Status Affected: Z

Description: The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed

in the ACC register.

Cycles: 1

IOST Load IOST Register

Syntax: IOST R Operands: R = 5 or 6

Operation: ACC → IOST register R

Status Affected: None

Description: IOST register 'R' (R= 5 or 6) is loaded with the contents of the ACC register.



MOVAR Move ACC to R

Syntax: MOVAR R Operands: $0 \le R \le 63$ Operation: ACC → R Status Affected: None

Description: Move data from the ACC register to register 'R'.

Cycles:

MOVIA Move Immediate to ACC

Syntax: MOVIA I Operands: 0≤1≤255 I → ACC Operation: Status Affected: None

Description: The 8-bit immediate '1' is loaded into the ACC register. The don't cares will assemble as 0s.

Cycles:

MOVR Move R

Syntax: MOVR R, d Operands: 0≤R≤63 $d \in [0,1]$

R → dest Operation:

Status Affected:

The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC Description:

register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since

status flag Z is affected.

Cycles: 1

NOP No Operation

NOP Syntax: Operands: None Operation: No operation Status Affected: None

Description: No operation.

Cycles:

OPTION Load OPTION Register

Syntax: **OPTION** Operands: None

Operation: ACC → OPTION

Status Affected: None

Description: The content of the ACC register is loaded into the OPTION register.

Cycles:

RETFIE Return from Interrupt, Set 'GIE' Bit

Syntax: RETFIE Operands: None

Top of Stack → PC Operation:

Status Affected: None

Description: The program counter is loaded from the top of the stack (the return address). The 'GIE' bit is

set to 1. This is a two-cycle instruction.



RETIA Return with Immediate in ACC

Syntax: RETIA I Operands: $0 \le I \le 255$ Operation: $I \to ACC$;

Top of Stack → PC

Status Affected: None

Description: The ACC register is loaded with the 8-bit immediate 'l'. The program counter is loaded from

the top of the stack (the return address). This is a two-cycle instruction.

Cycles: 2

RETURN Return from Subroutine

Syntax: RETURN Operands: None

Operation: Top of Stack \rightarrow PC

Status Affected: None

Description: The program counter is loaded from the top of the stack (the return address). This is a

two-cycle instruction.

Cycles: 2

RLR Rotate Left f through Carry

Syntax: RLR R, d Operands: $0 \le R \le 63$

d∈[0,1]

Operation: $R<7> \rightarrow C$;

 $R<6:0> \rightarrow dest<7:1>;$

 $C \rightarrow dest<0>$

Status Affected: C

Description: The contents of register 'R' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the

result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.

Cycles: 1

RRR Rotate Right f through Carry

Syntax: RRR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: $C \rightarrow dest<7>$;

 $R<7:1> \rightarrow dest<6:0>;$

R<0> → C

Status Affected: C

Description: The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the

result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.



SLEEP Enter SLEEP Mode

Syntax: SLEEP Operands: None

Operation: $00h \rightarrow WDT$;

00h → WDT prescaler;

 $1 \rightarrow \underline{TO}$;

 $0 \rightarrow \overline{PD}$

Status Affected: TO PD

Description: Time-out status bit (\overline{TO}) is set. The power-down status bit (\overline{PD}) is cleared. The WDT and its

prescaler are cleared.

The processor is put into SLEEP mode.

Cycles: 1

SBCAR Subtract ACC from R with Carry

Syntax: SBCAR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: $R + \overline{ACC} + C \rightarrow dest$

Status Affected: C, DC, Z

Description: Add the 2's complement data of the ACC register from register 'R' with Carry. If 'd' is 0 the

result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.

Cycles: 1

SUBAR Subtract ACC from R

Syntax: SUBAR R, d Operands: $0 \le R \le 63$

 $d\!\in\![0,\!1]$

Operation: $R - ACC \rightarrow dest$

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is

stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.

Cycles: 1

SUBIA Subtract ACC from Immediate

Syntax: SUBIA I
Operands: $0 \le I \le 255$ Operation: $I - ACC \rightarrow ACC$ Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is

placed in the ACC register.

Cycles: 1

SWAPR Swap nibbles in R

Syntax: SWAPR R, d Operands: $0 \le R \le 63$

 $d\!\in\![0,\!1]$

Operation: $R<3:0> \rightarrow dest<7:4>$;

R<7:4> \rightarrow dest<3:0>

Status Affected: None

Description: The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in

ACC register. If 'd' is 1 the result in placed in register 'R'.



XORAR Exclusive OR ACC with R

Syntax: XORAR R, d Operands: $0 \le R \le 63$

 $d \in [0,1]$

Operation: ACC xor $R \rightarrow dest$

Status Affected: Z

Description: Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in

the ACC register. If 'd' is 1 the result is stored back in register 'R'.

Cycles: 1

XORIA Exclusive OR Immediate with ACC

Syntax: XORIA I Operands: $0 \le I \le 255$

Operation: ACC xor I \rightarrow ACC

Status Affected: Z

Description: The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed

in the ACC register.



4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature 0°C to $+70^{\circ}\text{C}$ Store Temperature -65°C to $+150^{\circ}\text{C}$ DC Supply Voltage (Vdd) 0V to +6.0V Input Voltage with respect to Ground (Vss) -0.3V to (Vdd +0.3)V

5.0 OPERATING CONDITIONS

DC Supply Voltage +2.3V to +5.5V Operating Temperature 0°C to +70°C

6.0 ELECTRICAL CHARACTERISTICS

6.1 ELECTRICAL CHARACTERISTICS of FM8PS54E/S56E

To be defined

6.2 ELECTRICAL CHARACTERISTICS of FM8PS54/S56

Under Operating Conditions, at four clock instruction cycles and WDT & LVDT are disabled

Sym	Description	Conditions	Min.	Тур.	Max.	Unit	
_	X'tal oscillation range	HF mode, Vdd=5V	1		20	MHz	
F _{HF}	A tai oscillation range	HF mode, Vdd=3V	1		15	IVITZ	
_	V'4-1: -4:	LF mode, Vdd=5V	32		2000	1/117	
F_{LF}	X'tal oscillation range	LF mode, Vdd=3V	32		1000	KHZ	
_	DC coeilletion ronge	ERC mode, Vdd=5V	DC		15	MHz	
F _{ERC}	RC oscillation range	ERC mode, Vdd=3V	DC		7	IVIHZ	
		ERIC mode, external R, Vdd=5V	DC		15		
_	DO	ERIC mode, external R, Vdd=3V	DC		7	MHz	
F _{IRC/ERIC}	RC oscillation range	IRC mode, internal R, Vdd=5V		3.2		MHZ	
		IRC mode, internal R, Vdd=3V		3.2			
		I/O ports (except IOA4, IOA5), Vdd=5V	2.0				
		IOA4/T0CKI,IOA5/RSTB pins, Vdd=5V	4.0			,,	
V_{IH}	Input high voltage	I/O ports (except IOA4, IOA5), Vdd=3V	1.5			V	
		IOA4/T0CKI,IOA5/RSTB pins, Vdd=3V	2.4				
		I/O ports (except IOA4, IOA5), Vdd=5V			1.0		
		IOA4/T0CKI,IOA5/RSTB pins, Vdd=5V			1.0		
V_{IL}	Input low voltage	I/O ports (except IOA4, IOA5), Vdd=3V			0.6	V	
		IOA4/T0CKI,IOA5/RSTB pins, Vdd=3V			0.6		
V _{OH}	Output high voltage	I _{OH} =-5.4mA, Vdd=5V	3.6			V	
V _{OL}	Output low voltage	I _{OL} =8.7mA, Vdd=5V			0.6	V	
I _{PH}	Pull-high current	Input pin at Vss, Vdd=5V		-50		uA	
I _{PD}	Pull-down current	Input pin at Vdd, Vdd=5V		35		uA	
	WDT (Vdd=5V		4.7	7		
I _{WDT}	WDT current	Vdd=3V		0.7	2.5	uA	
		Vdd=3V		20.6			
T_{WDT}	WDT period	Vdd=4V		17.9		mS	
		Vdd=5V		15.8			
		Vdd=5V LVDT = 3.6V		23	35	_	
I _{LVDT}	LVDT current	Vdd=5V LVDT = 2V		11	20	uA	
		Vdd=3V LVDT = 2V		3.1	6.0		
		Sleep mode, Vdd=5V, WDT enable		5.9			
I_{SB}	Power down current	Sleep mode, Vdd=5V, WDT disable		1.3		uA	
		Sleep mode, Vdd=3V, WDT enable		1.2			
		Sleep mode, Vdd=3V, WDT disable		0.6		_	
I _{DD}	Operating current	HF mode, Vdd=5V, 4 clock instruction				mA	
		20MHz		1.76			
		15MHz		1.49			
		10MHz		1.15			



		4MHz	0.67	
		2MHz	0.53	
		HF mode, Vdd=3V, 4 clock instruction		
		20MHz	0.75	
	On a reation of a common t	15MHz	0.59	А
I_{DD}	Operating current	10MHz	0.46	mA
		4MHz	0.24	
		2MHz	0.15	
		HF mode, Vdd=5V, 2 clock instruction		
		20MHz	2.58	
	0	15MHz	2.06	0
I_{DD}	Operating current	10MHz	1.56	— mA
		4MHz	0.87	
		2MHz	0.70	
		HF mode, Vdd=3V, 2 clock instruction		
		20MHz	1.16	
	0	15MHz	0.90	\Box .
I_{DD}	Operating current	10MHz	0.65	m/
		4MHz	0.32	
		2MHz	0.19	
		LF mode, Vdd=5V, 4 clock instruction		
	Operating current	2MHz	157	
		1MHz	102	\neg
I_{DD}		500KHz	112	uA
		100KHz	45	
		32KHz	34	
		LF mode, Vdd=3V, 4 clock instruction		
		2MHz	67	
		1MHz	40	
I_{DD}	Operating current	500KHz	34	uA
		100KHz	10	
		32KHz	4.3	
		LF mode, Vdd=5V, 2 clock instruction		
		2MHz	250	
		1MHz	148	
I_{DD}	Operating current	500KHz	136	uA
		100KHz	48	
		32KHz	35	
		LF mode, Vdd=3V, 2 clock instruction		
		2MHz	113	
		1MHz	63	
I _{DD}	Operating current	500KHz	46	uA
		100KHz	13	
		32KHz	5	



		EDC mod	e, Vdd=5V, 4 cl	ack instruction	Ī		
		ERC IIIO0		1	F 620		
			R=1Kohm	F=32.72MHz	5.630		
		0.00	R=3.3Kohm	F=18.76MHz	2.313		
		C=3P	R=10Kohm	F=8.48MHz	0.930		
			R=100Kohm	F=1.06MHz	0.120		
			R=300Kohm	F=364KHz	0.047		
			R=1Kohm	F=22.08MHz	4.751		
			R=3.3Kohm	F=9.96MHz	1.681		
		C=20P	R=10Kohm	F=3.896MHz	0.610		
			R=100Kohm	F=436KHz	0.077		
I_{DD}	Operating current		R=300Kohm	F=148KHz	0.031		mA
			R=1Kohm	F=7.36MHz	3.802		
			R=3.3Kohm	F=2.668MHz	1.214		
		C=100P	R=10Kohm	F=940KHz	0.417		
			R=100Kohm	F=100KHz	0.052		
			R=300Kohm	F=33KHz	0.024		
			R=1Kohm	F=3.712MHz	3.371		
		C=300P	R=3.3Kohm	F=1.272MHz	1.058		
			R=10Kohm	F=440KHz	0.358		
			R=100Kohm	F=44KHz	0.043		
			R=300Kohm	F=15KHz	0.022		
		ERC mod	e, Vdd=3V, 4 clo				
		C=3P	R=1Kohm	F=18.84MHz	2.649		
			R=3.3Kohm	F=13.44MHz	1.092		
			R=10Kohm	F=7.52MHz	0.471		
			R=100Kohm	F=1.156MHz	0.062		
			R=300Kohm	F=412KHz	0.020		
			R=1Kohm	F=13.92MHz	2.460		
			R=3.3Kohm	F=8.2MHz	0.901		
		C=20P	R=10Kohm	F=3.74MHz	0.337		
			R=100Kohm	F=472KHz	0.037		
I_{DD}	Operating current		R=300Kohm	F=160KHz	0.013		mA
20			R=1Kohm	F=6.72MHz	2.188		
			R=3.3Kohm	F=2.844MHz	0.714		
		C=100P	R=10Kohm	F=1.068MHz	0.243		
			R=100Kohm	F=116KHz	0.026		
			R=300Kohm	F=40KHz	0.010		
			R=1Kohm	F=3.628MHz	2.048		
			R=3.3Kohm	F=1.368MHz	0.642		
		C=300P	R=10Kohm	F=492KHz	0.214		
		300.	R=100Kohm	F=52KHz	0.024		_
			R=300Kohm	F=17KHz	0.009		
I _{DD}	Operating current	FRC mod	e, Vdd=5V, 2 cl		0.000		mA
טטי	Sporading outlone	C=3P	R=1Kohm	F=31.74MHz	7.158		111/3
		0-35	R=3.3Kohm	F=18.7MHz	3.260		
			K-3.3KUIIII	Γ-10.7 IVIΠZ	 3.200		



	1		T		1	T	1
			R=10Kohm		1.356		
			R=100Kohr		0.173		
			R=300Kohr	n F=376KHz	0.067		
			R=1Kohm	F=21.88MHz	5.851		
			R=3.3Kohm	F=10.16MHz	2.194		
		C=20P	R=10Kohm	F=3.90MHz	0.810		
			R=100Kohr	n F=434KHz	0.097		
			R=300Kohr	n F=150KHz	0.040		
			R=1Kohm	F=7.32MHz	4.143		
			R=3.3Kohm	F=2.64MHz	1.340		
		C=100P	R=10Kohm	F=938KHz	0.460		
			R=100Kohr	n F=98KHz	0.054		
			R=300Kohr	n F=32KHz	0.025		
			R=1Kohm	F=3.72MHz	3.550		
			R=3.3Kohm	F=1.27MHz	1.115		
		C=300P	R=10Kohm	F=438KHz	0.378		
			R=100Kohr	n F=44KHz	0.047		
			R=300Kohr	n F=14KHz	0.024		
		ERC mode	e, Vdd=3V, 2	clock instruction			
			R=1Kohm	F=18.88MHz	3.265		
			R=3.3Kohm	F=13.22MHz	1.531		
		C=3P	R=10Kohm	F=7.56MHz	0.701		
			R=100Kohr	n F=1.086MHz	0.096		1
			R=300Kohr	n F=402KHz	0.035		
			R=1Kohm	F=14.1MHz	2.896		
			R=3.3Kohm	F=8.30MHz	1.151		
		C=20P	R=10Kohm	F=3.74MHz	0.443		
			R=100Kohr	n F=480KHz	0.052		
I_{DD}	Operating current		R=300Kohr	n F=160KHz	0.019		mA
			R=1Kohm	F=6.66MHz	2.410		
			R=3.3Kohm	F=2.82MHz	0.800		
		C=100P	R=10Kohm	F=1.062MHz	0.271		
			R=100Kohr	n F=116KHz	0.028		1
			R=300Kohr	n F=40KHz	0.011		1
			R=1Kohm	F=3.60MHz	2.156		1
			R=3.3Kohm	F=1.354MHz	0.687		1
		C=300P	R=10Kohm	F=488KHz	0.235		1
			R=100Kohr	n F=52KHz	0.023		1
			R=300Kohr	n F=18KHz	0.009		1
la-	Operating current	ERIC mod	le, external R	, Vdd=5V,			mA
I _{DD}	operating current	4 clock ins					'''^
		R=47Kohr	n F=	:18.5MHz	2.375		



		R=100Kohm	F=9.2MHz	1.310	
		R=300Kohm	F=3.1MHz	0.478	
		R=470Kohm	F=2.0MHz	0.317	
		R=1Mohm	F=950KHz	0.154	
		R=2Mohm	F=480KHz	0.074	
		R=5.1Mohm	F=190KHz	0.029	
		R=10Mohm	F=100KHz	0.0145	
		R=20Mohm	F=50KHz	0.0074	
			ernal R, Vdd=3V,	0.007 1	
		4 clock instructio			
		R=47Kohm	F=16.0MHz	0.960	
		R=100Kohm	F=8.8MHz	0.612	
		R=300Kohm	F=3.1MHz	0.238	
I_{DD}	Operating current	R=470Kohm	F=2.0MHz	0.157	mA
		R=1Mohm	F=950KHz	0.076	
		R=2Mohm	F=480KHz	0.037	
		R=5.1Mohm	F=190KHz	0.0143	
		R=10Mohm	F=100KHz	0.0074	
		R=20Mohm	F=50KHz	0.0038	
		ERIC mode, exte	ernal R,Vdd=5V,		
		2 clock instructio	n		
		R=47Kohm	F=18.5MHz	3.457	
		R=100Kohm	F=9.1MHz	1.928	
		R=300Kohm	F=3.1MHz	0.713	
I_{DD}	Operating current	R=470Kohm	F=2.0MHz	0.471	mA
		R=1Mohm	F=950KHz	0.230	
		R=2Mohm	F=480KHz	0.114	
		R=5.1Mohm	F=190KHz	0.044	
		R=10Mohm	F=100KHz	0.0221	
		R=20Mohm	F=50KHz	0.0113	
		ERIC mode, exte 2 clock instructio			
		R=47Kohm	F=16.0MHz	1.550	
		R=100Kohm	F=8.8MHz	0.960	
		R=300Kohm	F=3.1MHz	0.366	
I _{DD}	Operating current	R=470Kohm	F=2.0MHz	0.241	mA
		R=1Mohm	F=950KHz	0.118	
		R=2Mohm	F=480KHz	0.058	
		R=5.1Mohm	F=190KHz	0.0225	
		R=10Mohm	F=100KHz	0.0115	
		R=20Mohm	F=50KHz	0.0060	
I _{DD}	Operating current	IRC mode, interr	nal R, Vdd=5V,		mA
טטי	Sporating ouriont	F=3.2MHz		0.388	



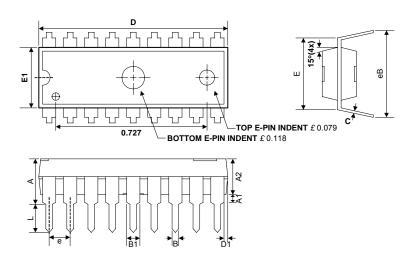
I _{DD} Operating current		IRC mode, internal R, Vdd=3V, 4 clock instruction		mA
	F=3.2MHz	0.187		
I _{DD}	Operating current	IRC mode, internal R,Vdd=5V, 2 clock instruction		mA
		F=3.2MHz	0.527	
I _{DD}	Operating current	IRC mode, internal R,Vdd=3V, 2 clock instruction		mA
		F=3.2MHz	0.263	





7.0 PACKAGE DIMENSION

7.1 18-PIN PDIP 300mil

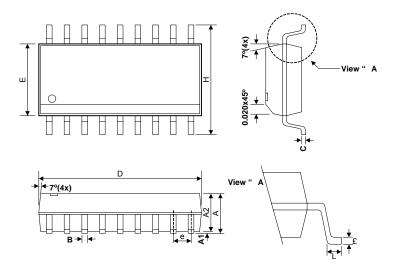


Cumph ala	Dime	Dimension In Millimeters			Dimension In Inches		
Symbols	Min	Nom	Max	Min	Nom	Max	
А	-	-	4.57	-	=	0.180	
A1	0.13	-	-	0.005	-	=	
A2	-	3.30	3.56	-	0.130	0.140	
В	0.36	0.46	0.56	0.014	0.018	0.022	
B1	1.27	1.52	1.78	0.050	0.060	0.070	
С	0.20	0.25	0.33	0.008	0.010	0.013	
D	22.71	22.96	23.11	0.894	0.904	0.910	
D1	0.43	0.56	0.69	0.017	0.022	0.027	
E	7.62	-	8.26	0.300	-	0.325	
E1	6.40	6.50	6.65	0.252	0.256	0.262	
е	-	2.54	-	-	0.100	-	
L	3.18	-	-	0.125	-	-	





7.2 18-PIN SOP 300mil

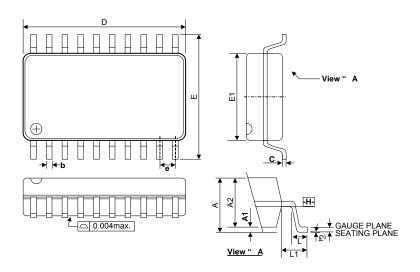


Cumphala	Dimension In Millimeters		eters	Dimension In Inches		
Symbols	Min	Nom	Max	Min	Nom	Max
А	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.04	-	0.012
A2	-	2.31	-	-	0.091	-
В	0.33	0.41	0.51	0.013	0.016	0.020
С	0.18	0.23	0.28	0.007	0.009	0.011
D	11.35	-	11.76	0.447	-	0.463
Е	7.39	7.49	7.59	0.291	0.295	0.299
е	-	1.27	-	-	0.050	-
Н	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
θ	0°	-	8°	0°	-	8°





7.3 <u>20-PIN SSOP 209mil</u>



O. mala ala	Dimension In Millimeters				
Symbols	Min	Nom	Max		
А	-	-	2.00		
A1	0.05	-	-		
A2	1.65	1.75	1.85		
b	0.22	-	0.38		
С	0.09	-	0.21		
D	6.90	7.20	7.50		
Е	7.40	7.80	8.20		
E1	5.00	5.30	5.60		
е	-	0.65	-		
L	0.55	0.75	0.95		
L1	-	1.25	-		
θ°	0°	4°	8°		



ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size
FM8PS54EP	PDIP	18	300 mil
FM8PS54ED	SOP	18	300 mil
FM8PS54ER	SSOP	20	209 mil
FM8PS56EP	PDIP	18	300 mil
FM8PS56ED	SOP	18	300 mil
FM8PS56ER	SSOP	20	209 mil

Mask Type MCU	Package Type	Pin Count	Package Size
FM8PS54P	PDIP	18	300 mil
FM8PS54D	SOP	18	300 mil
FM8PS54R	SSOP	20	209 mil
FM8PS56P	PDIP	18	300 mil
FM8PS56D	SOP	18	300 mil
FM8PS56R	SSOP	20	209 mil